

REMARKS/ARGUMENTS

The rejections presented in the Office action dated September 27, 2005 have been considered. Claims 1-17 are pending in the application. According to the Office Action, Claims 1-17 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. § 112, second paragraph. The conditional allowability of Claims 1-17 is acknowledged, and the Applicant thanks the Examiner for favorable consideration of these claims. Reconsideration of the pending claims and allowance of the application in view of the present amendment and response is respectfully requested.

The Specification is objected to because, according to the Examiner, the title of the invention is excessive. In order to facilitate prosecution of the Application, the Applicant has amended the specification in response to the objection so that the title now reads "Simultaneous Serial Transmission of Messages with Data Field Arbitration." Applicant respectfully requests withdrawal of the objection.

Claims 1-17 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Applicant respectfully traverses the rejection. The Examiner states that, in regard to a report message group (RMG):

[T]he specification describes sending the report messages in a RMG according to a protocol designed to assure all of them will be sent by all of the data processors DP1, etc. involved in perfect synchronism (See page 24, lines 22-23 and page 25, line 1.) If the report messages are transmitted at the same time with the same number of bytes, it is unclear how one would resolve ownership of the bus to complete transmission. Further explanation and clarification is requested. (Office Action, paragraph 3).

The Applicant respectfully submits that the present Specification describes resolving bus ownership in a way as to enable one skilled in the art to make or use the invention. First, Applicant notes that in the embodiments described in the Specification, that the first bits of *all* transmitted messages are sent at the same time in response to particular events, regardless of whether or not the message is part of a RMG. For example:

It is important that the new report query message or *any other message* sent by another node 10, etc. be started in rigid synchronism relative to the end of the previous message. In one protocol, each node 10, etc. waits three bit times after the end of a message before attempting to send another message. (page 18, lines 1-5)(emphasis added)

Therefore, in the arbitration scheme described in the Specification to support Claims 1-17, any two or more nodes that simultaneously desire to send a message will send their first bit at the same time, e.g., three bit times after the end of a previous message. The ownership of the bus is thereafter resolved during message transmission by the nodes themselves using bitwise arbitration. Bitwise arbitration is described in the following excerpts from the present Specification:

A problem recognized for a very long time is that of message collisions, where two or more nodes send messages on the signal wires at the same time. One solution is that of the CAN (controller area network) system. In the CAN system, messages are encoded in binary signals that are either dominant or recessive bits. If a node sends a dominant bit signal, the dominant bit is present on the signal path regardless of the number of recessive bits sent by other nodes. Each node senses the signal on the signal path, and ceases sending its message if, when sending a recessive bit, the node senses a dominant bit. This process of each node detecting collisions in real time and ceasing message sending upon detecting a collision is called arbitration. The CAN system is explained in more detail in U. S. Patent Nos. 5,001,642 and 5,303,348.

Typically, each type of message has a unique leading ID portion. This assures that eventually only one message survives arbitration. The node sending the surviving message continues sending until the message is completed, at which time all of the nodes wait for a short period of time, and then as many as have messages to send, start sending new messages. (page 3, lines 17-23 and page 4, lines 1-8).

Each of the data processors DP1, etc. is programmed to stop further transmission of bit values when the signal on path DATI does not agree with the signal on path DATO. This process of continually testing by each transmitting node 10, 30, etc., as to whether the signal on line 15 agrees with the signal that data processor DP1 is transmitting through transmitter 11, is called arbitration. One can see that as signal transmission continues in real time, more and more of any transmitting nodes 10, 30, etc. will stop transmitting as they lose arbitration by transmitting a recessive bit while another node 10, 30, etc. is transmitting a dominant bit. Eventually, a single transmitting node 10, 30, etc. wins arbitration and it will transmit to the end of its message because there is no longer an opportunity for another node 10, 30, etc. to win arbitration during a bit time. (page 13, lines 9-18).

Therefore, in response to the Examiner's question about how one resolves ownership of the bus to complete transmission, the answer is that ownership is resolved through bitwise arbitration. However, there is an additional consideration regarding synchronization of messages in the case of RMG messages. Recall that RMG messages are designed to allow the determination of a maximum or minimum value reported from all of the nodes of a RMG (see, e.g., page 5, lines 4-10). Note that all messages within an RMG will have identical

leading bits up until the DATA field associated with the RMG (page 25, lines 8-11 and FIG. 2A). The data field contains the value of interest (e.g., temperature, pressure, etc.) for each node (e.g., page 10, line 23 to page 11, lines 1-2). As a result, arbitration between RMG messages will be won based on the value of the DATA fields in the RMG messages, and not based on the header fields preceding the DATA, because the bits of those header fields are the same for all messages of the RMG. Thus of all the RMG messages being transmitted, only one message will win arbitration, that message being the one with the greatest number of leading dominant bits in its DATA field. Because the DATA bits are used to form a binary number in order from leading to trailing bits, the DATA value that wins arbitration is the one with the highest or lowest numeric value (lowest if a transformation such as bitwise inversion is performed on the value). This is explained in the present Specification as follows:

This protocol assures three important results. First, the priority of each of the report messages in a RMG is identical through all of the bits preceding the DATA field, which assures that all of them will eventually be sent simultaneously without any losing arbitration until at least the first bit of the DATA field is sent. Secondly, these report messages will all win or lose arbitration simultaneously with respect to every message that is in a SMQ but is not in the particular RMG. Third, when the reports in a RMG win arbitration through the DATA LGT field, further arbitration on the individual report messages' bits will be based on the bits in the DATA fields. These results may seem to be obvious, but they are an important feature that must be grasped for the following description to be understood. When all of the nodes 10, etc. use the AC power wave on line 16 to synchronize in all of the nodes 10, etc., each of the bit times and the messages that the bit times form, then a high degree of synchronism among the report messages occurs. By causing each of the data processors DP1, etc. to follow the message selection and sending protocols, the communication system of which nodes 10, etc. form a part, can in essence become a distributed wired OR logic network, *allowing only the one or more report messages in a RMG having the largest or smallest of the DATA fields to win arbitration through the end of the message.* (page 25, lines 7-23)(emphasis added)

Therefore, the "perfect synchronism" as noted by the Examiner relates to the synchronism of nodes sending an RMG message at the same time in response to a particular event (e.g., in response to a query as described on page 18, lines 9-12). In that case, all of the RMG messages should be sent at the same time after the event, and if a node loses arbitration of its RMG message to another RMG message of the same group, the losing node does not need to retransmit (see, e.g. page 36, lines 17-21, "[a]ll of the messages in the particular RMG will then be removed from their nodes' SMQs at nearly the same time" after only one RMG

message wins arbitration). In this way, the value of interest (e.g., the highest or lowest DATA value of all RMG messages) can be communicated in the time it takes to send only a single message, instead of requiring all of the RMG nodes to send their messages in separate time slots, after which the maximum/minimum DATA values could be determined.

Thus, Applicant respectfully submits that the present Specification describes the bus arbitration in such a way as to enable one skilled in the art to make or use the invention, and thus satisfies the requirement of 35 U.S.C. § 112, first paragraph. Applicants also note that the language of Claims 1-17 contains language related to the bitwise arbitration described above. For example, Claim 1 sets forth “wherein each node while sending senses the signal level on the data path during each bit interval, and if the sensed signal level differs from that sent by that node, halts further sending of signal levels by that node.” As to the particular claim language referred to in the rejection, the Applicant notes that “providing the send signal to the message sending module” is described in the present Specification on page 36, lines 17-23 through page 37, lines 1-10. Therefore, Applicant respectfully submits that the Specification fully enables one skilled in the pertinent art to make and use the subject matter of Claims 1-17. In light of this, Applicant respectfully requests withdrawal of the rejection.

Claims 1-17 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter. In particular, the Examiner objects to the terms “encoding a node data value,” as well as other uses of the term “encoding” in the claims, stating that “it is well-known in the art that processors perform encoding, not signals.” The Examiner also alleges that the “content of the *node data value* is unclear from the claim.” (emphasis in original). Applicants respectfully traverse the rejection.

As to the term “node data value,” the Applicants submit that “data value” is a term well known in the art. In the context of the claims, the node data value is any data associated with each of the first and second nodes (e.g., Claim 1, lines 11-12) that is encoded in low order bits of a report message (e.g., Claim 1, lines 20-24). As to the term “encoding,” the Applicants respectfully submit that signals may be used to encode data values and fields, thus the use of the term “encoding” is proper in this context. However, in order to facilitate prosecution, Applicant has amended Claims 1 and 10 to replace the term “encoding” with

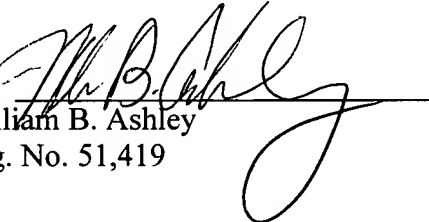
“representing” to more clearly describe the relationship between the signals and the data. Applicants respectfully submit that the amendments made to Claims 1 and 10 and the remarks hereinabove overcome the rejections made under 35 U.S.C. § 112, second paragraph, and therefore place Claims 1-17 in condition for allowance. Applicants also note that these amendments are not made for purposes relating to patentability, and are not made in response to prior art or any objections or rejections to the claims. Thus, the Applicant has not intended to narrow, nor has the Applicant narrowed, the scope of any of the claims resulting from the amendment.

If the Examiner believes it necessary or helpful, the undersigned agent of record invites the Examiner to contact him at 952.854.2700 to discuss any issues related to this case.

Respectfully submitted,

HOLLINGSWORTH & FUNK, LLC
8009 34th Avenue South, Suite 125
Minneapolis, MN 55425

Date: January 25, 2006

By: 
William B. Ashley
Reg. No. 51,419